Serial Number: 09/592,009 Filing Date: June 12, 2000

Title: CONTEXT SWITCH ARCHITECTURE AND SYSTEM

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## **REMARKS**

Applicant has carefully reviewed and considered the Office Action mailed on May 23, 2006, and the references cited therewith.

Claims 1 and 8 have been amended, and new claims 15-20 have also been added. As a result, claims 1-20 are now pending in this application.

 $T = -\frac{1}{2} \mathcal{F}(\theta, \theta) + \frac{1}{2} \mathcal{F}(\theta, \theta)$ 

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## Double Patenting Rejection and Objection to Declaration

Claims 1-13 were provisionally rejected under the judicially created doctrine of double patenting over claims 1, 4-5 of co-pending Application No. 11/314,036 in view of *Maupin*. A terminal disclaimer, if necessary, will be filed when an indication of allowable subject matter is received.

Also, the Office Action has objected to the Declaration as being defective. A substitute Declaration will be filed upon receipt of a Notice of Allowance.

## \$103 Rejection of the Claims

Claims 1-13 were rejected under 35 USC § 103(a) as being unpatentable over *Maupin* (U.S. Patent 6,154,832). Applicant disagrees with these rejections because *Maupin* does not teach or suggest the subject matter of amended claim 1 or claim 8. Applicant requests withdrawal of the rejections and allowance of the claims.

Claim 1 as amended recites in pertinent part:

A method of performing a context switch operation, comprising:

accessing context data in a first register of a peripheral system when a context index is set to a first index value;

receiving, by the peripheral system, a second index value from a host computer associated with the peripheral system;

setting the context index to the second index value to perform a context switch; accessing context data in a second register of the peripheral system when the context index is set to the second index value, wherein the first and second registers are collocated with the peripheral system.

(Emphasis Added)

Respectfully, *Maupin* does not teach or suggest providing a first or second register collocated with a peripheral system. Applicant's application describes that there is no need for context information to be transferred from the host computer to the peripheral system each time a context switch occurs. Such a transfer slows down the context-switch operation and burdens the network with transmission of context information.

In stark contrast, *Maupin* shows that processor (12) includes register file (44), and thus the register file is collocated with processor (12) and therefore not with a peripheral system as required by claim 1. *Maupin* relates to the use of multiple register sets in a processor in order to eliminate the need for interrupts. Interrupt sources may record interrupt service requests instead of signaling an interrupt to the processor. Periodically, the processor may poll service request registers (34A-34F) to determine if a service request is recorded. The processor (12) includes a register file (44) that includes multiple register sets (46A-46H) within its register file such that a different register set may be permanently assigned to tasks corresponding to each of the interrupt sources.

Execution core 40 determines which register set (46A-46H) from which to access the register. Task ID register 42 may store a value indicative of the task currently executing. Task

IDs may be assigned to each interrupt source. Upon initiation of a particular task, the task ID identifying that task is stored in task ID register 42. Execution core 40 uses the value stored in task ID register 42 to select a register set (46A-46H) within register file 44, and used the register number from a particular instruction to select a particular register within that register set.

Thus Maupin does not teach or suggest an architecture in which a register file is collocated with a peripheral system. For at least these reasons, claim 1 is allowable because Maupin does not disclose all the elements of claim 1.

Claims 2-7 depend from claim 1 and are allowable for the reasons claim 1 is allowable. Claim 8 includes limitations similar to claim 1. Thus, for at least the reasons stated above with respect to claim 1, claim 8 is allowable. Claims 9-13 depend from claim 8 and are allowable for at least the reasons claim 8 is allowable.

New claims 15-20 have also been added and are believed to be patentable over the cited art.

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## Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (703-286-5303) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521.

Respectfully submitted,

Brake Hughes PLC Customer Number 57246 703-286-5303

Date September 25, 2006

R. Edward Brake Reg. No. 37,784

<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, <u>VA 22313-1450</u>, on this <u>25th</u> day of September, 2006.

Shellie Bailey

Cellie Bailey
Signature